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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,009	03/07/2005	Fransiscus Jacobus Vossen	NL 020817	1122

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
HO, BAO QUAN T	
ART UNIT	**PAPER NUMBER**
2609	
MAIL DATE	**DELIVERY MODE**
08/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/527,009	VOSSEN ET AL.	
	Examiner	Art Unit	
	Bao-Quan T. Ho	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1 and 7** are rejected under 35 U.S.C. 102(b) as being anticipated by Ide et al., US Patent 6,304,038 (hereafter referenced as Ide).

3. **Regarding claim 1,** Ide discloses a matrix display device having row electrodes (Xn and Yn in fig. 3) and column electrodes (Zn in fig. 3), an intersection of a row and a column electrode defining a pixel cell (col. 4 lines 14-25) having a pixel cell capacitance (C0 in fig. 4), and drive circuits (30, 40, 50) for driving the row electrodes (Xn and Yn in fig. 3) and the column electrodes (Yn in fig. 3) including means for discharging at least partially the pixel cell capacitance (C0 in fig. 4) through an inductor (L2 in fig. 4) into a buffer capacitor (C1 in fig. 4), thereby storing energy from the pixel cell capacitance (C0 in fig. 4) into the buffer capacitor (C1 in fig. 4), characterized in that the drive circuits (30, 40 and 50 in fig. 4) include means for discharging at least partially the buffer capacitor (C1 in fig. 4) through a means for controlling (S1 in fig. 4) an amount of

electrical charge into the pixel cell capacitance (C0 in fig. 4), thereby recovering at least partially the stored energy (col. 5 lines 46-51).

4. **Regarding claim 7,** Ide discloses a method of driving a matrix display having row electrodes (Xn and Yn in fig. 3) and column electrodes (Zn in fig. 3), an intersection of a row and a column electrode defining a pixel cell (col. 4 lines 14-25) having a pixel cell capacitance (C0 in fig. 4), the method including a first step of discharging at least partially the pixel cell capacitance (C0 in fig. 4) through an inductor (L2 in fig. 4) into a buffer capacitor (C1 in fig. 4), characterized in that the method includes a further step of discharging at least partially the buffer capacitor (C1 in fig. 4), through a means for controlling an amount of electrical charge (S1 in fig. 4) flowing into the pixel cell capacitance (C0 in fig. 4, col. 5 lines 46-51).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 2-4, 8, and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ide, in view of Sano et al., US Patent 7,078,865 (hereafter referenced as Sano).

7. **Regarding claim 2**, Ide does not specifically teach a matrix display device characterized in that the means for controlling an amount of electrical charge flowing into the pixel cell capacitance is a current source. However, Sano teaches a power

distributing means, that is a current source (22 in fig. 5) (col. 2 lines 32-39), inserted between a driving power supply (1 in fig. 5) and driving device (6 in fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Ide's apparatus to insert a power distributing means (Sano, 22 in fig. 5), that is a current source, between the power supply circuit (Ide, 21 in fig. 4) and pixel data pulse generating circuit (Ide, 22 in fig. 4) as taught by Sano for the purpose of reducing the power consumed in the capacitive load, as well as simplifying the heat sinking structure to reduce circuit cost (col. 8 lines 52-60).

8. **Regarding claim 3**, combination of Ide and Sano teach everything as applied above in claim 2. The combination also teaches the display device further having a power supply (Ide, B1 in fig. 4) adapted to deliver power to the pixel cell (Ide, C0 in fig. 4) through the current source (Sano, 22 in fig. 5).

9. **Regarding claim 4,** combination of Ide and Sano teach everything as applied above in claim 3. The combination also teaches a matrix display device characterized in that the buffer capacitor (Ide, C1 in fig. 4) has one terminal connected to the inductor (Ide, L1 in fig. 4) and another terminal connected to ground (Ide, Vs in fig. 4).

10. **Regarding claim 8,** combination of Ide and Sano discloses a method of driving a matrix display device characterized in that the means for controlling an amount of electrical charge flowing into the pixel cell capacitance is a current source (Sano, 22 in fig. 5).

11. **Regarding claim 9,** combination of Ide and Sano discloses a method of driving a matrix display further having a power supply (Ide, B1 in fig. 4) adapted to deliver power to the pixel cell (Ide, C0 in fig. 4) through the current source (Sano, 22 in fig. 5).

12. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ide, in view of Cheng, US Patent 6,819,308.

13. **Regarding claim 5,** The combination does not specifically teach a matrix display device characterized in that the buffer capacitor has a capacitance which is comprised between 10 and 100 times the sum of the pixel cell capacitances of all pixel cells of the display device. However, Cheng teaches a matrix display with the ratio of the storage capacitance to the maximum panel capacitance should be at least about 10:1 and preferably at least about 20:1, and most preferably 30:1 (col. 7 lines 30-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Ide's apparatus to have the buffer capacitor have a capacitance which is comprised between 10 and 100 times the sum of the pixel cell capacitances of all pixel cells of the display device as taught by Cheng for the purpose of conserving power depending on the size of the display panel, whether it be a heavy panel load, average panel load, or a light panel load (col. 7 lines 30-50).

14. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ide, in view of Kim et al., US Patent 6,451,456 (hereafter referenced as Kim).

15. **Regarding claim 6,** Ide does not specifically teach a matrix display characterized in that the display device is of the organic luminescent type. However, Kim discloses the use of organic electroluminescence devices can be used as a pixel of a graphic display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Ide's apparatus to use organic electroluminescence as pixel for the matrix display device as taught by Kim for the purpose of wide viewing angle, fast response speed, and high contrast (col. 1 lines 33-42)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao-Quan T. Ho whose telephone number is (571) 270-3264. The examiner can normally be reached on M-F, 7:30 am to 5:00 pm EST, alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian T. Pendleton can be reached on (571) 272-7527. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH
08/06/07

BRIAN TYRONE PENDLETON
SUPERVISORY PATENT EXAMINER